ABSTRACT OF THE DISCLOSURE

Provided is a data processor capable of preferentially starting an interrupt processing when an interrupt request occurs during burst transfer to cache memory. When an interrupt request (IR) is detected during burst transfer to an instruction cache (3), the instruction cache (3) suspends the burst transfer and creates break information (35). Upon return to the original program at the termination of the interrupt processing, the instruction cache (3) restarts the burst transfer from the suspended point by referring to a restart address described in an address description part (35a) of the break information (35).